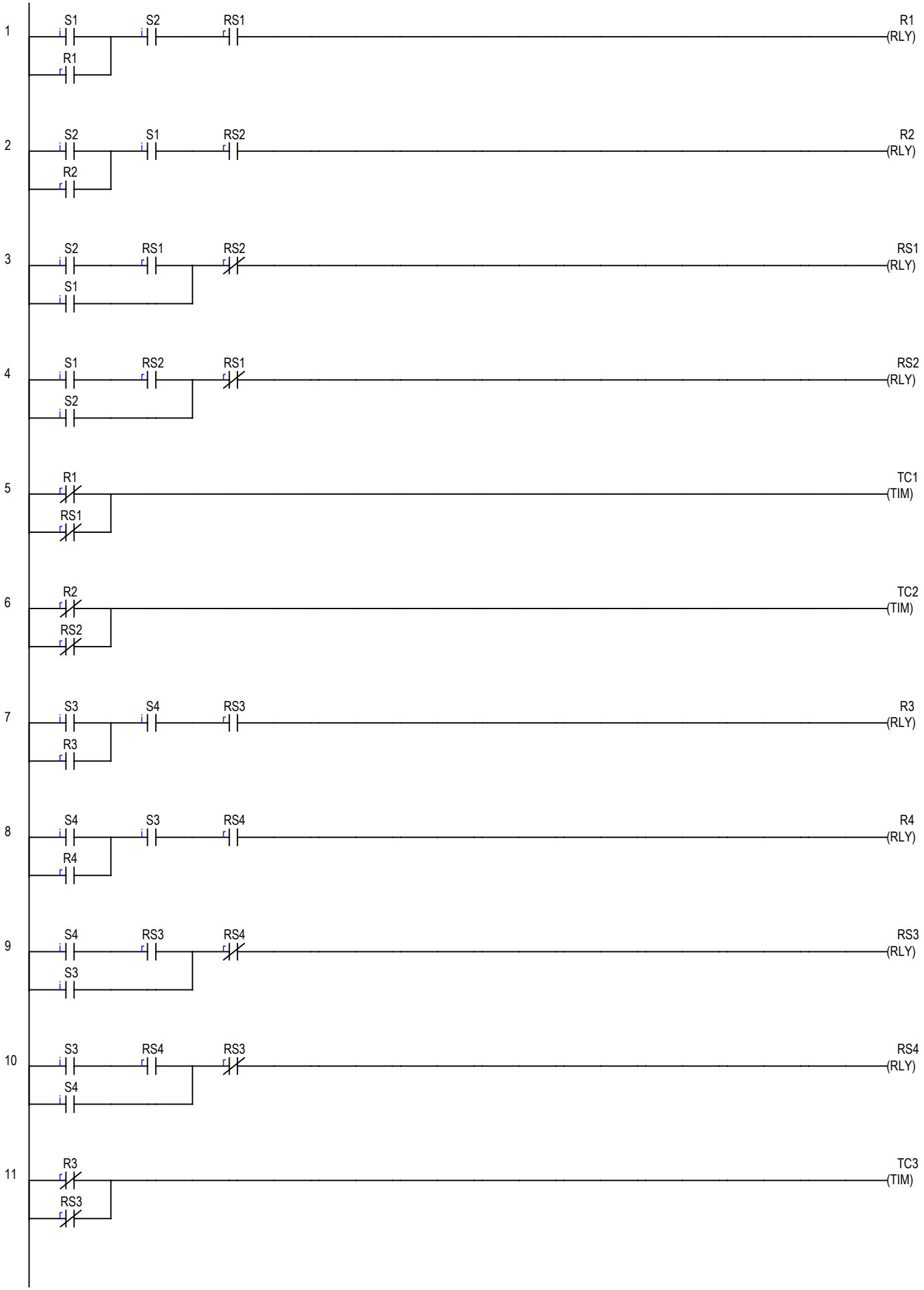
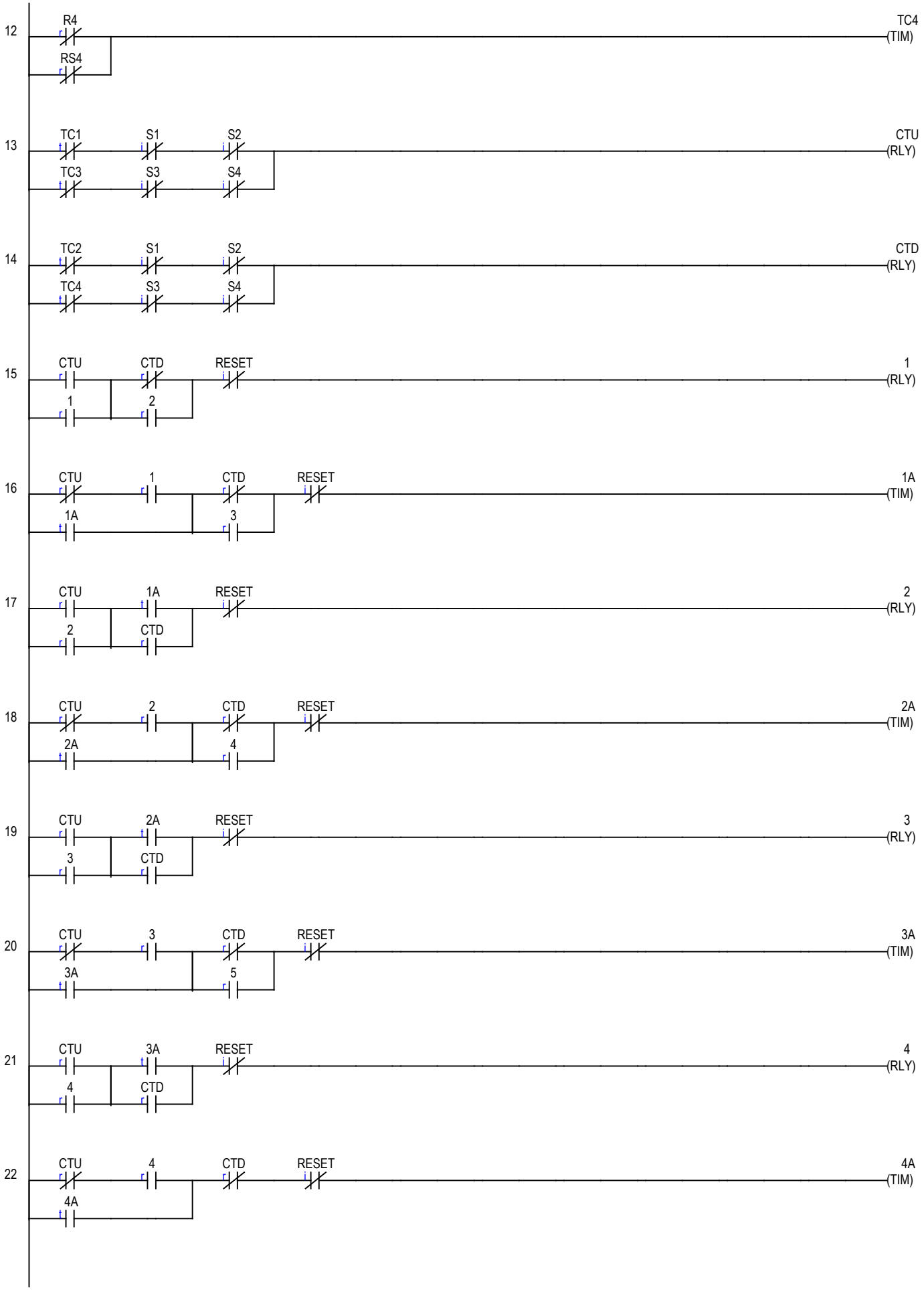
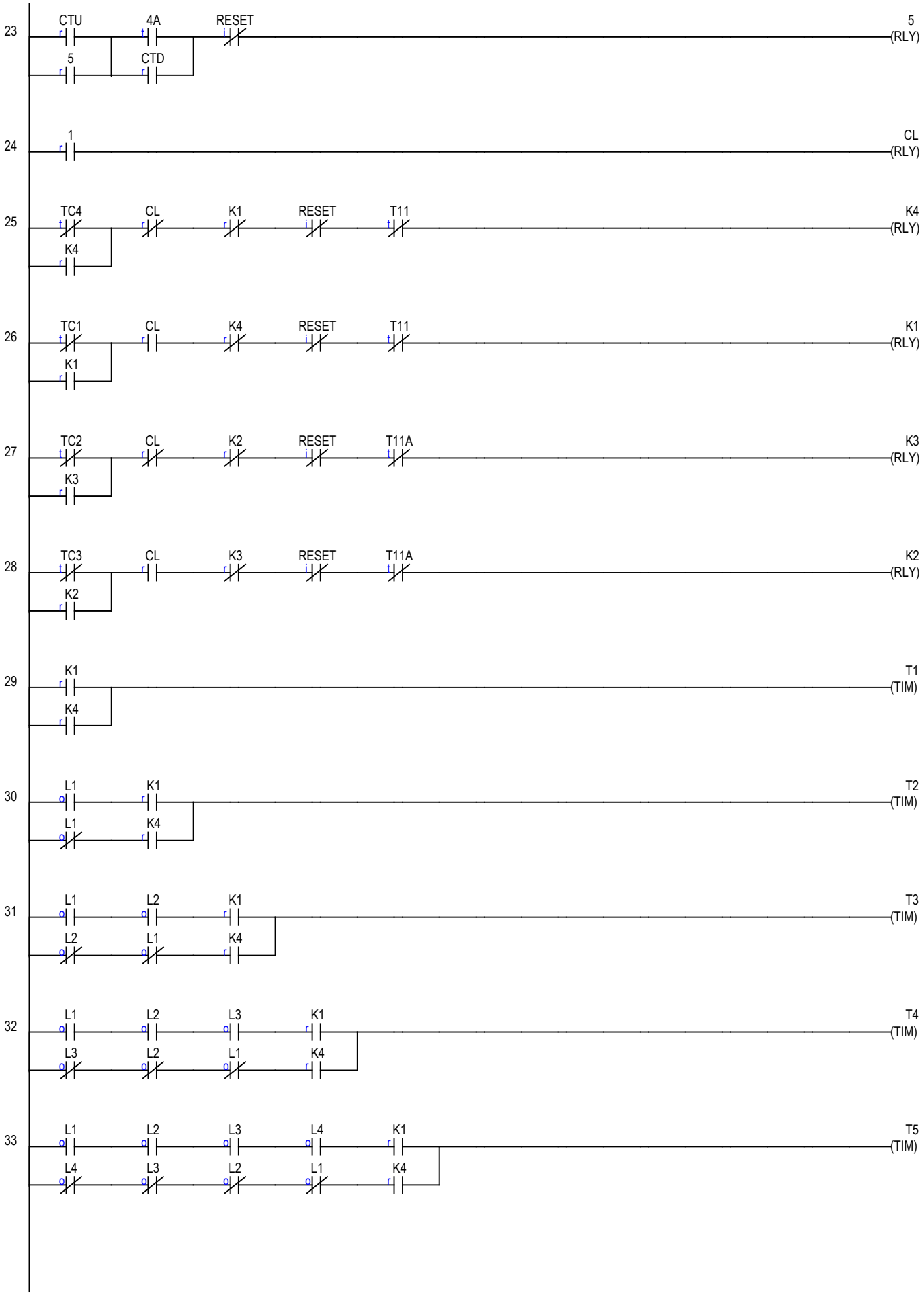
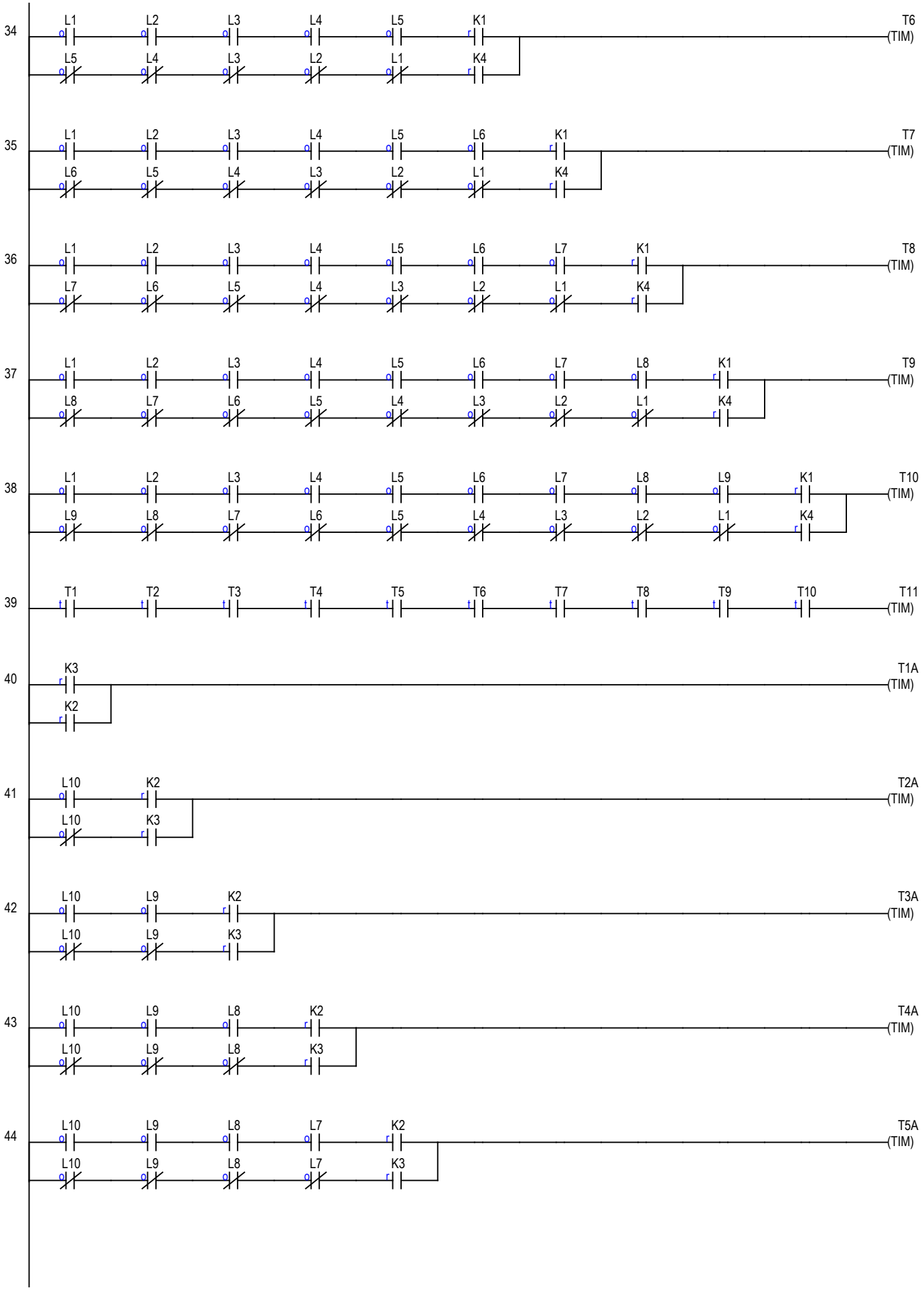
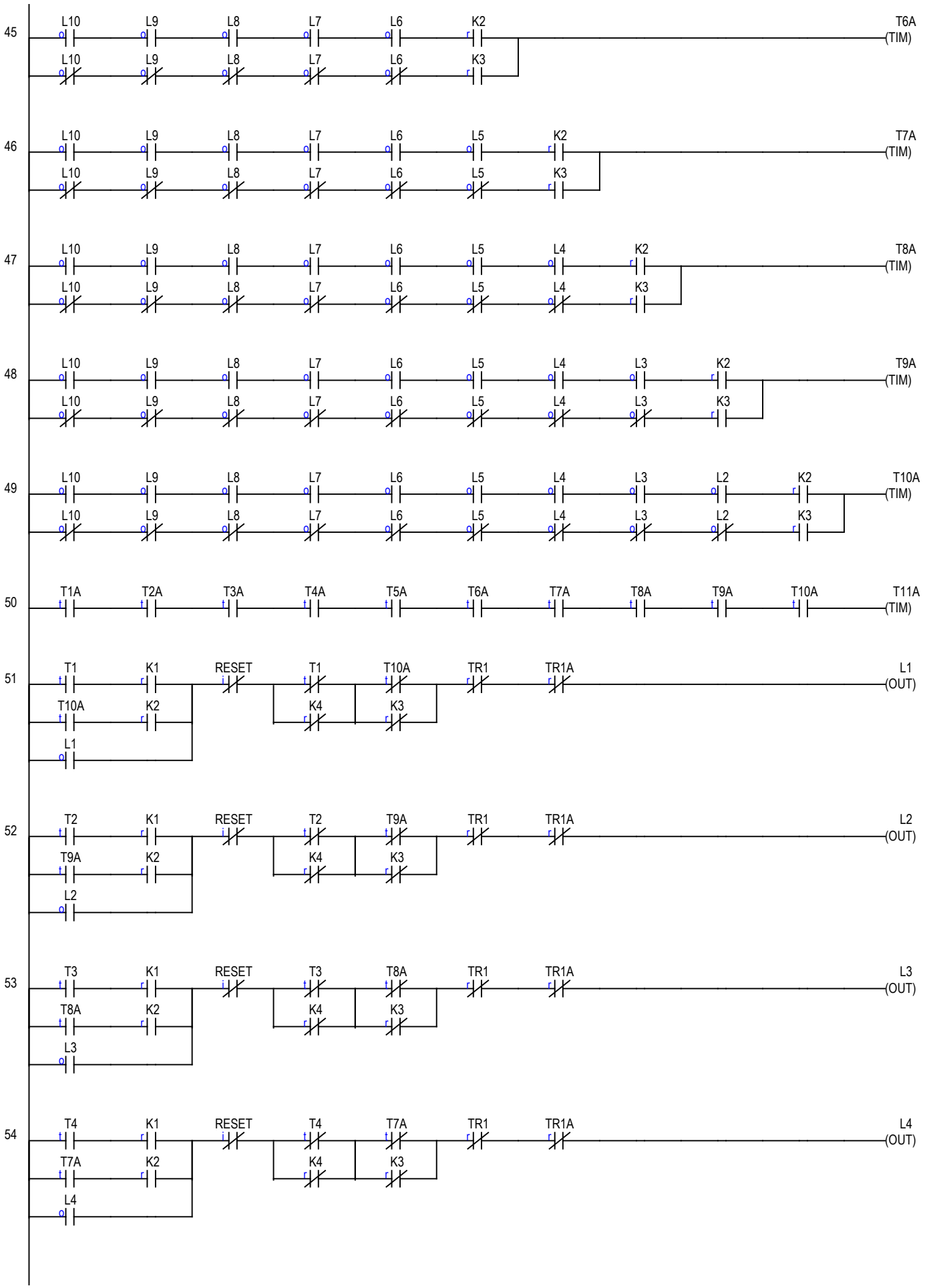
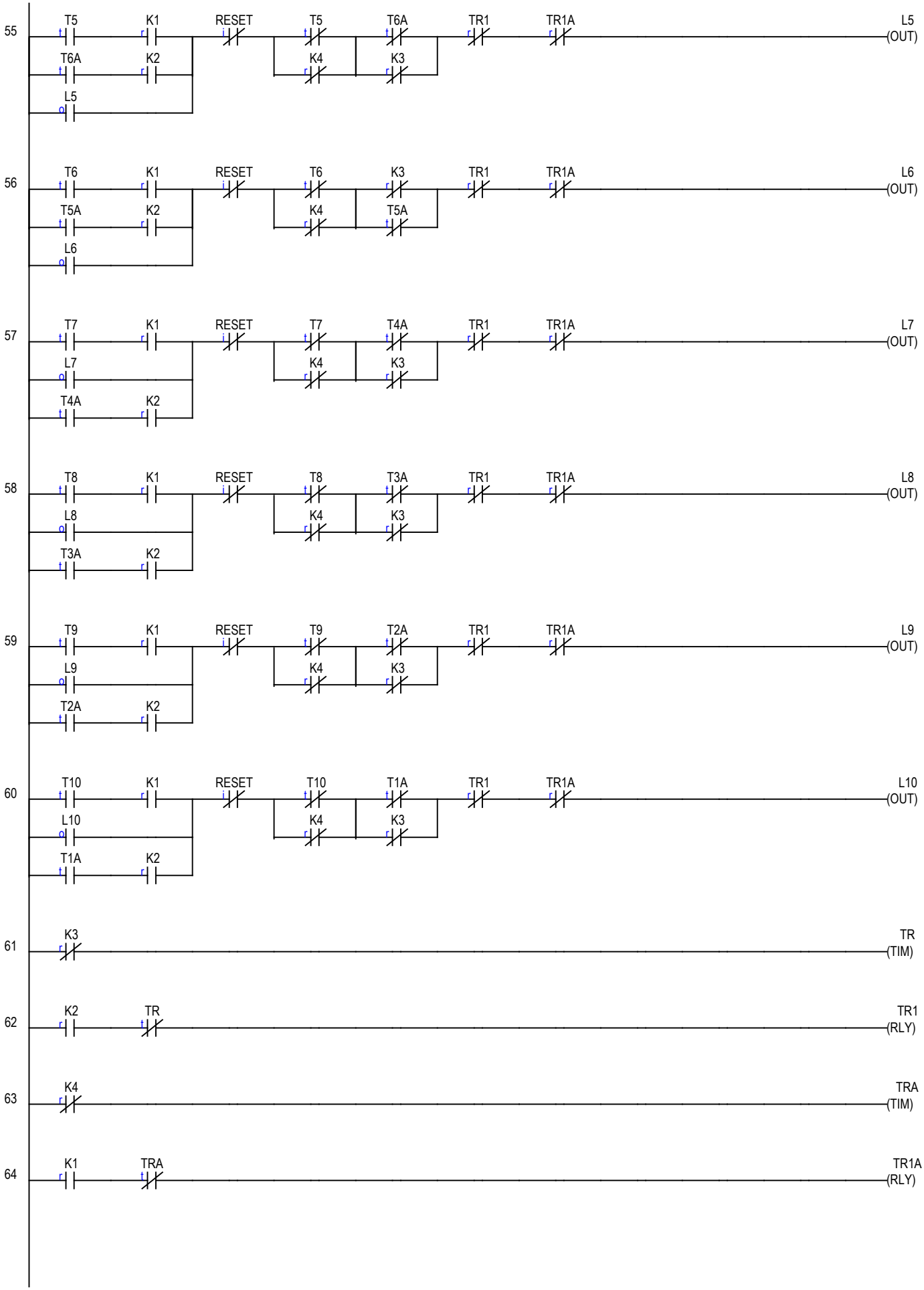

1
S1
S2
RS1
R1
R1
(RLY)
2
S2
S1
RS2
R2
R2
(RLY)
3
S2
RS1
RS2
S1
RS1
(RLY)
4
S1
RS2
RS1
S2
RS2
(RLY)
5
R1
RS1
TC1
(TIM)
6
R2
RS2
TC2
(TIM)
7
S3
S4
RS3
R3
R3
(RLY)
8
S4
S3
RS4
R4
R4
(RLY)
9
S4
RS3
RS4
S3
RS3
(RLY)
10
S3
RS4
RS3
S4
RS4
(RLY)
11
R3
RS3
TC3
(TIM)


12
R4
RS4
TC4
(TIM)
13
TC1
S1
S2
TC3
S3
S4
CTU
(RLY)
14
TC2
S1
S2
TC4
S3
S4
CTD
(RLY)
15
CTU
CTD
RESET
1
2
1
(RLY)
16
CTU
1
CTD
RESET
1A
3
1A
(TIM)
17
CTU
1A
RESET
2
CTD
2
(RLY)
18
CTU
2
CTD
RESET
2A
4
2A
(TIM)
19
CTU
2A
RESET
3
CTD
3
(RLY)
20
CTU
3
CTD
RESET
3A
5
3A
(TIM)
21
CTU
3A
RESET
4
CTD
4
(RLY)
22
CTU
4
CTD
RESET
4A
4A
(TIM)


23
CTU
4A
RESET
5
(RLY)
5
CTD
24
1
CL
(RLY)
25
TC4
CL
K1
RESET
T11
K4
(RLY)
K4
26
TC1
CL
K4
RESET
T11
K1
(RLY)
K1
27
TC2
CL
K2
RESET
T11A
K3
(RLY)
K3
28
TC3
CL
K3
RESET
T11A
K2
(RLY)
K2
29
K1
T1
(TIM)
K4
30
L1
K1
T2
(TIM)
L1
K4
31
L1
L2
K1
T3
(TIM)
L2
L1
K4
32
L1
L2
L3
K1
T4
(TIM)
L3
L2
L1
K4
33
L1
L2
L3
L4
K1
T5
(TIM)
L4
L3
L2
L1
K4


34
L1 L2 L3 L4 L5 K1
L5 L4 L3 L2 L1 K4
T6 (TIM)
35
L1 L2 L3 L4 L5 L6 K1
L6 L5 L4 L3 L2 L1 K4
T7 (TIM)
36
L1 L2 L3 L4 L5 L6 L7 K1
L7 L6 L5 L4 L3 L2 L1 K4
T8 (TIM)
37
L1 L2 L3 L4 L5 L6 L7 L8 K1
L8 L7 L6 L5 L4 L3 L2 L1 K4
T9 (TIM)
38
L1 L2 L3 L4 L5 L6 L7 L8 L9 K1
L9 L8 L7 L6 L5 L4 L3 L2 L1 K4
T10 (TIM)
39
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10
T11 (TIM)
40
K3
K2
T1A (TIM)
41
L10 K2
L10 K3
T2A (TIM)
42
L10 L9 K2
L10 L9 K3
T3A (TIM)
43
L10 L9 L8 K2
L10 L9 L8 K3
T4A (TIM)
44
L10 L9 L8 L7 K2
L10 L9 L8 L7 K3
T5A (TIM)


45
L10 L9 L8 L7 L6 K2
L10 L9 L8 L7 L6 K3
T6A (TIM)
46
L10 L9 L8 L7 L6 L5 K2
L10 L9 L8 L7 L6 L5 K3
T7A (TIM)
47
L10 L9 L8 L7 L6 L5 L4 K2
L10 L9 L8 L7 L6 L5 L4 K3
T8A (TIM)
48
L10 L9 L8 L7 L6 L5 L4 L3 K2
L10 L9 L8 L7 L6 L5 L4 L3 K3
T9A (TIM)
49
L10 L9 L8 L7 L6 L5 L4 L3 L2 K2
L10 L9 L8 L7 L6 L5 L4 L3 L2 K3
T10A (TIM)
50
T1A T2A T3A T4A T5A T6A T7A T8A T9A T10A
T11A (TIM)
51
T1 K1 RESET T1 T10A TR1 TR1A
T10A K2 K4 K3
L1
L1 (OUT)
52
T2 K1 RESET T2 T9A TR1 TR1A
T9A K2 K4 K3
L2
L2 (OUT)
53
T3 K1 RESET T3 T8A TR1 TR1A
T8A K2 K4 K3
L3
L3 (OUT)
54
T4 K1 RESET T4 T7A TR1 TR1A
T7A K2 K4 K3
L4
L4 (OUT)


55
T5
K1
RESET
T5
T6A
TR1
TR1A
L5
(OUT)
T6A
K2
K4
K3
L5
56
T6
K1
RESET
T6
K3
TR1
TR1A
L6
(OUT)
T5A
K2
K4
T5A
L6
57
T7
K1
RESET
T7
T4A
TR1
TR1A
L7
(OUT)
L7
K4
K3
T4A
K2
58
T8
K1
RESET
T8
T3A
TR1
TR1A
L8
(OUT)
L8
K4
K3
T3A
K2
59
T9
K1
RESET
T9
T2A
TR1
TR1A
L9
(OUT)
L9
K4
K3
T2A
K2
60
T10
K1
RESET
T10
T1A
TR1
TR1A
L10
(OUT)
L10
K4
K3
T1A
K2
61
K3
TR
(TIM)
62
K2
TR
TR1
(RLY)
63
K4
TRA
(TIM)
64
K1
TRA
TR1A
(RLY)